Sparrow MEMs Microphone with Programmable Gain & Activity Detector

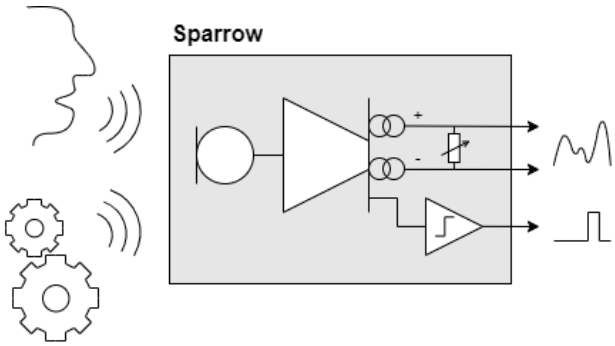
General description

The Sparrow device is a MEMS microphone with analog signal output, acoustic activity detection and adjustable signal gain. An interrupt line can notify or wake up a host controller whenever the acoustic activity exceeds a selectable threshold.

The signal output is implemented with a pair of complementary current sources, which makes the device compatible with differential signal receivers and also single ended receivers, having a voltage input or a current input. In addition to the built in adjustable resistors, an external resistor can be used to flexibly set the voltage gain.

This makes the device particularly suitable as sensor frontend for automated acoustic monitoring systems which need to be permanently listening, supporting the requirement to save power by reducing the average up-time of controlling units further down the signal chain, and offering the flexibility to dynamically adapt to changes in environmental acoustic conditions.

Diagram



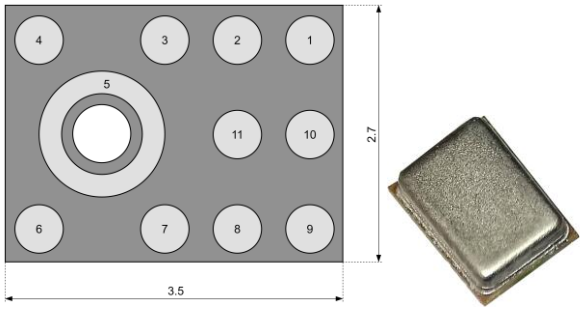
Features

- Acoustic activity detection with adjustable threshold level and frequency characteristic
- Analog output current pair providing a differential or a single ended signal
- Wide gain adjustment range with internal programmable resistors, and/or external resistors
- Sensitivity selection range exceeding -50...0 dBV at 94dB$_{SPL}$
- SPI interface and interrupt line
- Current consumption 19µA
- single 1.8V supply
- SNR 53dB$_{A}$, AOP 120dB$_{SPL}$
- Package 3.5x2.7mm with acoustic bottom port

Applications

- Always-listening monitoring and surveillance for maintenance, safety or entertainment
- First level detection stage in acoustic event recognition systems
- Automatic gain control (AGC) audio systems
- Keyword spotting applications

Package illustration



Contents

1. Overview

1.1 Document revision history

Revision	Comments	Author	Date
0	IC datasheet and product brief created	Matthias Steiner	9-July-2024
1.0	Compiled prerelease document	David Schie	21-Aug-2024
1.1	Prerelease optimization	Matthias Steiner	28-Aug-2024

1.2 Purpose

This document describes how to operate Sparrow, which is a low power MEMS microphone device with voice activity detection VAD and configurable gain.

1.3 Block diagram

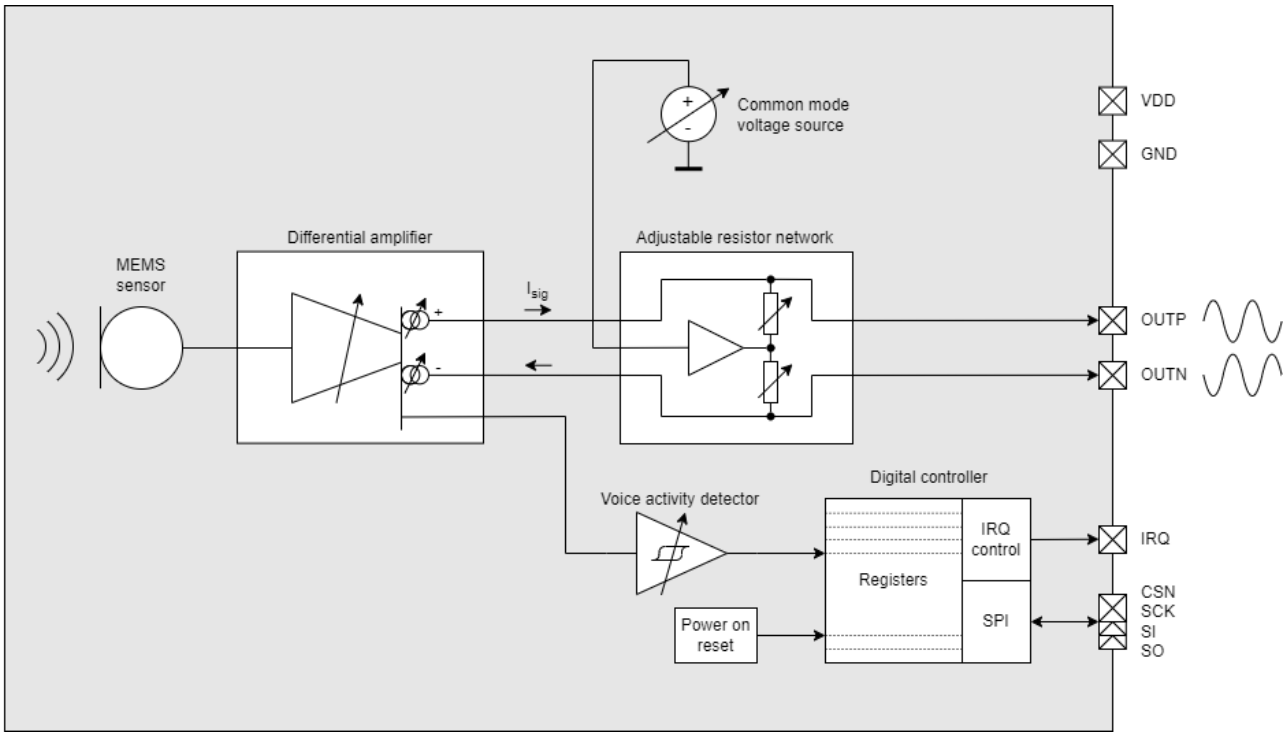


Figure 1 Sparrow block diagram

2. Absolute maximum ratings

The absolute maximum ratings are stress ratings only, functional operation is not implied. Exposure to these conditions for extended periods may affect device reliability and shorten lifetime.

Parameter	Value	Note
Supply from VDD to GND	-0.3V … +3V	
Pad voltage at OUTN, OUTP, SO, SI, SCLK, CSN, FLAG4	GND-0.3V … VDD+0.3V	
Pad voltage at IRQ	GND-0.3V … 8V	
Max DC current at OUTN, OUTP, SO, VDD, SI, SCLK, GND, IRQ, CSN, FLAG4	+-25mA	
ESD robustness	2kV HBM	JEDEC JS-001
Latchup robustness	+-100mA	JEDEC JESD78

Table 1 Absolute maximum ratings

3. Characteristics

Parameter	min	typ	max	Unit	Note
Supply voltage	1.6	1.8	2.0	V	At 1.6V some features might be degraded, e.g. large signal THD.
Operating temperature	0	25	70	°C	Package temperature
SPI clock speed			40	MHz	

Table 2 Conditions

Parameter	min	typ	max	Unit	Note
idd	14	19	39	µA	
idd_pd		0.4		µA	Power down mode
total mic sensitivity, default settings		-34		dBV/Pa	Adjustable, see register settings for fe_gain, fe_idis, rselp, rseln
Output resistors, default settings	170	232 (116+116)	290	kΩ	Total active resistance between OUTP, OUTN
DC output offset	-35		+35	mV	
SNR		53		dB_A	A-weighted, at $94dB_{SPL}$
THD		0.3		%	At $94dB_{SPL}$, 1kHz
AOP		120		dB_{SPL}	Acoustic overload point (10% distortion)
VAD threshold, vthsel=0		69		dB_{SPL}	acoustic sine wave signal
VAD threshold, vthsel=7		104		dB_{SPL}	like above, but another threshold setting

Table 3 Characteristics with default gain settings

4. Digital functions

4.1 SPI interface

Features:

- SPI interface with 3 byte transmission to read (or read&write) one SPI register location, see timing diagram in Figure 2.
- The first bit selects if the transmission is going to be only a read (WN=1) or a read&write (WN=0) transmission.
- Data is sampled by the IC with the rising SCLK edge, and changed at the falling SCLK edge
- SCLK may be low or high at the CSN transition (i.e. SPI mode 0 and 3 is supported, but not mode 1 and 2)
- 15 bit address (32768 register space)
- Burst operation: if the SPI master extends the transmission to more than 3 bytes, this will execute repeated reads (or read&writes) to the same register, and can for example be used to poll a status bit.
- The internal register state for the 8 bits of a register gets updated at the 23rd rising edge of SCLK

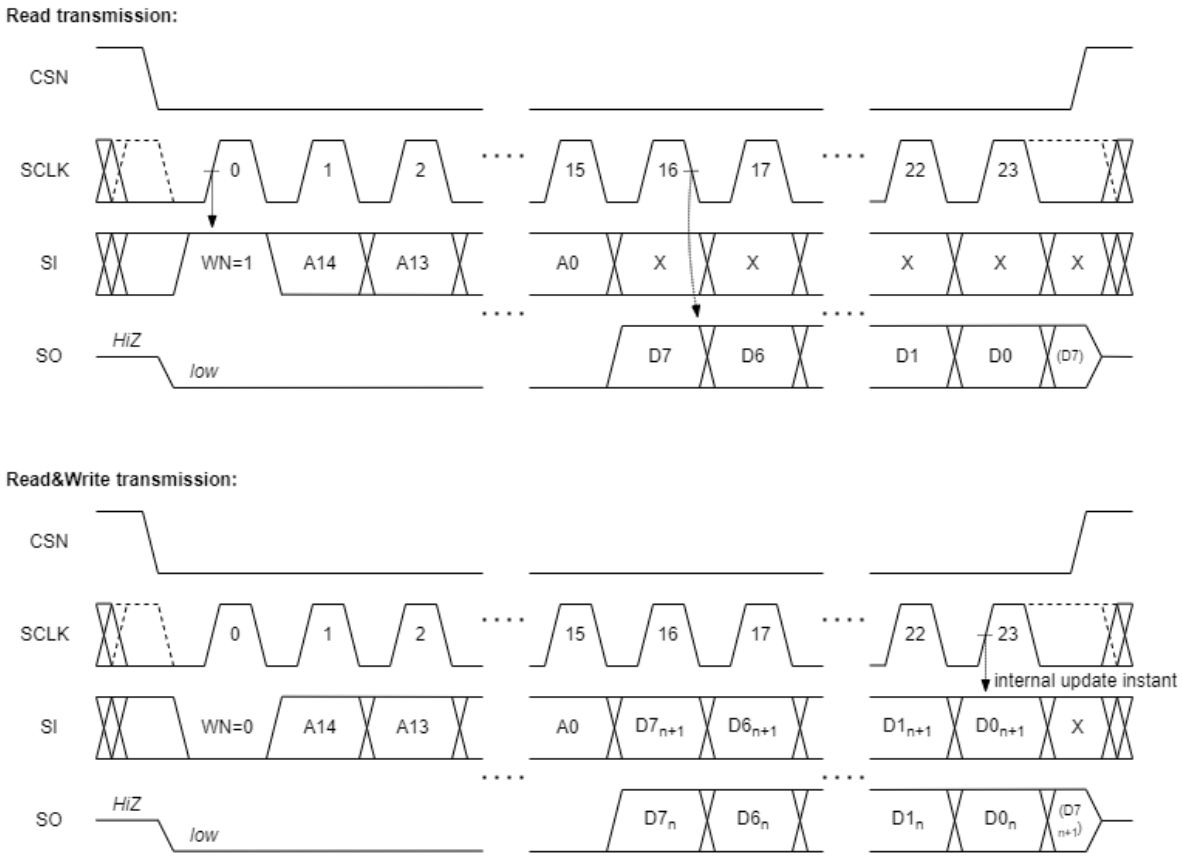


Figure 2 SPI transmission: read (top), read&write (bottom)

4.2 Register map

Table 4 shows the register map.

- Unused bits in used addresses should be masked to 0 when writing, unless stated otherwise
- Unused addresses should not be written to
- Reset state is 0, unless stated otherwise

Address	Name	Description
0x0000	siliconid	Device version identifier. Reading gives an 8 bit hard-coded number.
0x0002	wr_ctrl	bit[6] … irq_hiz, disables the IRQ digital output driver making the pad high-z
0x0003	irqstat	Interrupt status register Reading returns the interrupt status of each source (fired=1). Writing a "1" to a bit location clears the respective interrupt(s). The bits are activated by the respective interrupt source. bit[2] … nvmdone: gets fired if the internal boot operation after power up has completed (boot takes less than 0.3ms) bit[1] … vad: gets fired if voice activity is detected bit[0] … reset: gets fired at a power-up reset.
0x0004	irqen	Interrupt enable register. Each bit allows to enable an interrupt source. If left at 1, the interrupt function of that source is enabled and the interrupt status is forwarded to the IRQ pad. If set to 0: IRQ pad stays low for that source (note that, internally, the irqstat register still can get active for that source, only the forwarding to the IRQ pad is disabled). Reset state: 0x07 (i.e. all interrupts enabled). bit[2] … nvmdone bit[1] … vad bit[0] … reset
0x0010	pd	Power down control. Set the register to 0xFF to switch off the device, set back to 0x00 (default) for normal operation.
0x0012	config2	bit[7:5] … to be left at zero bit[4:0] … adj_amp, device output common mode voltage vcmout setting, encoding is two's complement (-16 … +15), vcmout=0.73V+adj_amp*19.1mV

0x0015	config5	Controls the number of active output current source units. This defines the signal gain in a wide range with fine granularity. Selectable are 0,1,2, …, 193 units. Setting control bits to high is disabling the respective units, e.g. 0x00 gives 193 active units, 0xFE gives 1 active unit. Per default, 16 units are active (reset value 0xEF). Note that, additionally, the gain can be adjusted with fe_gain and rselp/n (see below), which further extends the range of selectable gain settings. bit[7] … fe_idis66, disables a block of additional 66 units bit[6:0] … fe_idis, disable 0 to 127 units (binary encoding)
0x0016	config6	bit[6:5] … fe_gain, selects the amplifier gain in 6dB steps. Note that when changing fe_gain, fe_lowgmsel must be set to the same value as fe_gain. Encoding of fe_gain: 0x0: gain -6dB 0x1: gain 0dB (default) 0x2: gain +6dB 0x3: gain +12dB bit[4:3] … fe_lowgmsel, configures an internal amplifier regulation loop. Must be set to the same value as fe_gain. bit[2:0] … must always be left at 0x7 (all 3 bits high) when writing to this register

0x0017	config7	bit[5:3] … fzsel, selects the VAD low pass filter corner frequency. Encoding of fzsel: 0x0 … corner frequency 2Hz 0x1 … corner frequency 4Hz 0x2 … corner frequency 8Hz 0x3 … corner frequency 16Hz 0x4 … corner frequency 31Hz 0x5 … corner frequency 63Hz 0x6 … corner frequency 125Hz 0x7 … corner frequency 250Hz (default) bit[2:0] … vthsel, selects the VAD trigger threshold voltage in 6dB steps. The lower the setting, the more sensitive the VAD. The VAD threshold is scaling with the fe_gain setting, and is not affected by the fe_idis, rselp, rseln settings. Encoding of vthsel: 0x0 … nominal 0.78% 0x1 … nominal 1.56% 0x2 … nominal 3.13% 0x3 … nominal 6.25% 0x4 … nominal 12.5% 0x5 … nominal 25% 0x6 … nominal 50% 0x7 … nominal 100% (default)
0x0018	config8	bit[5:3] … rselp, selects the output resistor between OUTP and the internal common mode node. This affects the output impedance and the signal gain. Encoding of rselp: 0x0 … "0" Ω (<2k) 0x1 … 0.125x Rnom (14.5k) 0x2 … 0.25x Rnom (29k) 0x3 … 0.5x Rnom (58k) 0x4 … 1x Rnom (116k) (default) 0x5 … 2x Rnom (232k) 0x6 … 4x Rnom (464k) 0x7 … inf (for external resistors or current receivers) bit[2:0] … rseln, like rselp but resistor between OUTN and the internal common mode node. Usually, rseln would be set to the same value as rselp to get a symmetrical differential output voltage.

0x0019	config9	bit[6] … csn_pullu, enables a pullup resistor at CSN bit[5] … sclk_pulld, enables a pulldown resistor at SCLK bit[4] … so_pulld, enables a pulldown resistor at SO bit[3] … must be written to with 1 bit[2] … si_pulld, enables a pulldown resistor at SI bit[1] … irq_pulld, enables a pulldown resistor at IRQ bit[0] … irq_drvweak, reduces the driver strength of the IRQ pad digital output driver to 35%

Table 4 Register map

5. Package

Pad number	Pad name	Function
8	VDD	Positive supply
5+11	GND	Negative supply (ground). The two pads are shorted in the device.
2	CSN	SPI chip select input, active low
1	SCLK	SPI clock input
10	SI	SPI slave data input
9	SO	SPI slave data output (or high-z)
3	IRQ	Interrupt output, active high
7	OUTP	Amplifier output (positive)
6	OUTN	Amplifier output (negative)
4	FLAG4	placeholder for future use, should be left unconnected

Table 5 Pad list

Parameter	Value
x size	3.5 mm
y size	2.65 mm
height	1.0 mm

Table 6 Package dimensions

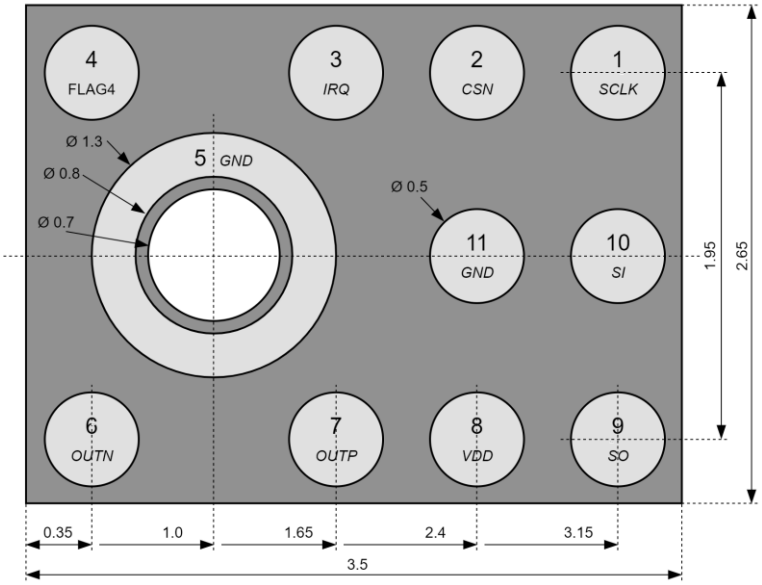


Figure 3 Pad location and sizes, top view “through” the device, unit is millimeters